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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,058	12/16/2003	James W. Nicholes	1280-SC12980TC	5196

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EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/737,058	NICHOLES, JAMES W.	
	Examiner	Art Unit	
	Tan T. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-23* is/are allowed.

6)☒ Claim(s) *1-9,12 and 23* is/are rejected.

7)☐ Claim(s) *10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/03, 04/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The Information Disclosure Statements submitted by Applicant on December 16, 2003 and April 5, 2004 have been received and fully considered.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5, 8-9, 12 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Hanriat et al. (U.S. Patent No. 6,282,114).

Regarding claims 1 and 23, Hanriat et al. disclosed in Figure 2 a ROM comprising a plurality of memory cells [MN] coupled between a plurality of word lines [W0-Wn] and a plurality of bit lines [BL], a plurality of reference cells (not shown) coupled to a reference bit line [DBL] (column 3, lines 5-10). A plurality of PMOS transistors [MP1, MP2] coupled between the bit lines [BL] and reference bit line [DBL] and high supply potential [Vdd] (column 2, line 66 to column 3, line 4). A plurality of NMOS transistors [MN1] coupled between the bit lines [BL], the reference bit line [DBL] and the low supply potential (ground) (column 3, lines 11-16). Hanriat et al. further disclosed in Figure 3 a timing diagram of a read operation of the ROM. A read signal [W], a clock signal [S] for sense amplifier [12], a [PUP] and [PDN] signals are generated by a sequencer [20] (column 3, lines 18-26). The [PUP*] signal is complement of signal [PUP] which is active when low, therefore, the signal [PUP*] is active when high (column 3, lines 27-31). In Figure 3, Hanriat et al. showed that as the read signal [W] goes low, which would be understood as the claimed inactive memory access period,

the signal [PDN] becomes high and the transistors [MN1] is ON to discharge the bit lines [BL] and reference bit line [DBL]. As a read operation starts, the selected bit line and the reference bit line is charging when the signal [PUP*} is high, and the difference of voltage between the selected bit line [BL] and the reference bit line [DBL] is sensed by the sense amplifier [12] (column 3, lines 49-67).

Regarding claim 2-3, as shown in Figure 3, the signal [S] to activate the sense amplifier [12] goes high after a delay as to the charging pulse [PUP*] goes high, and the [PUP*] has a pulse width, Hanriat et al. also disclosed the duration of activation signal [PUP*] as well as the features of transistors [MP1], [MP2] are chosen so that the level difference obtained in the read operation is sufficient to switch the sense amplifier (column 3, lines 52-55).

Regarding claim 4-5 and 12, as shown in Figure 3, the signal [S] to activate the sense amplifier goes high after a delay in respect to the charging signal [PUP*], the delay time is sufficient for the voltage on the selected bit line and the reference bit line [DBL] to be charged toward the stored value in the selected cell and the reference voltage [Vref].

Regarding claim 8, as shown in Figure 3, for the read operation of each memory cell, a charging pulse is applied to both the bit line [BL] and the reference bit line [DBL].

Regarding claim 9, as shown in Figure, after the read operation of each selected cell, a discharging pulse [PDN] is applied to both the bit line and the reference bit line [DBL].

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanriat et al..

Regarding claims 6-7, Hanriat did not disclose the voltage difference is greater than 100 or 150 mV. Hanriat disclosed the voltage difference is approximately 50 mV (column 4, lines 28).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the ROM of Hanriat et al. by selecting the voltage difference in the range of greater than or equal 100 or 150 mV.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to select the voltage difference in the range of greater than or equal 100 or 150 mV to obtain an accurate reading operation.

6. Claims 10-11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 13-23 are allowed.

The following is an examiner's statement of reasons for allowance: The prior art failed to show or suggest the drawing the voltage on the selected bit line and the

reference line to a midpoint voltage level as in claims 10-11. The prior art also failed to show or suggest the combination of a plurality of pass gate transistors configured to select one of the plurality of bit lines as a sensed node and a pull-up transistor coupled to the sense node as in claims 13-23.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

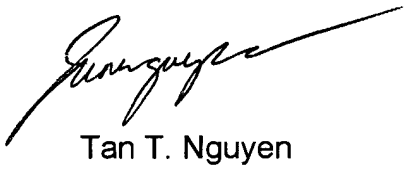
Matsumoto et al., Chang et al., and Semi are cited to show memory devices having discharge circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen
Primary Examiner
Art Unit 2827
June 16, 2005